An alternative to Reed-Solomon codes for forward error correction on optical channels

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ABSTRACT

In this paper, forward error correction schemes are discussed for application in the multigigabit-per-second optical channel. The proposed schemes, based on specific convolutional codes which allow simple decoding techniques, represent a valid alternative, in terms of performance and complexity, to the recommended Reed-Solomon codes.

Keywords: Forward error correction, Convolutional codes, Concatenated coding.

1. INTRODUCTION

Forward error correction (FEC) is a well established technique which may provide coding gain in long, optically amplified, digital transmission systems, to increase amplifier spacing or system capacity. In the multigigabit-per-second optical fiber submarine cable systems, the Reed-Solomon (RS) code (255,239) is recommended for its good trade-off between performance and complexity.[1] This code is also a candidate as an international standard in the network node interface (NNI) between administrative domains in terrestrial optical transport networks (OTN)[2]

A feature of RS codes is their capability of correcting bursts of errors.[3] However, up to now bursty errors have hardy ever been reported in high bit-rate, optically amplified systems. For instance, the errors generated in single-channel transmission systems limited by amplified spontaneous emission (ASE) noise and group velocity dispersion (GVD) are almost perfectly random.[4] In polarization mode dispersion (PMD) limited high-speed optical transmission systems with fluctuating differential group delay (DGD), the error distribution is not random.[5] Long sequences of errors may be actually generated by PMD—in this case the condition of random errors may be obtained providing sufficient interleaving only.[6] Being the coherence time of PMD phenomenon of the order of minutes or even longer, however sufficient interleaving is totally impractical to realize. Therefore, even in this case the correction capability of RS codes is insufficient and specific PMD compensators must be adopted.

As a valid alternative to RS codes, a convolutional self-orthogonal code (CSOC) with a simpler decoding scheme may therefore be adopted.[3,7–10] These codes are based on a particular algebraic property from which some important advantages derive: i) simple implementation of the encoder and decoder, in particular with majority-logic and threshold decoding, therefore operating at very high speed, and ii) the property of not producing additional and bursty errors at the output of the decoder when the capability of the decoder is exceeded.[7–10] Whilst the former property, which determined the interest for these codes in satellite communications in the Sixties and Seventies,[8–10] is now appealing in the high-speed optical channel,[11,12] the latter becomes essential if the code is going to be used in a concatenated scheme, where some of the most powerful decoders, such as those for RS codes or the Viterbi algorithm, exhibit additional uncorrectable errors of a bursty nature at their output.

In this paper, we propose some simple, high rate, FEC solutions based on CSOCs and majority-logic/threshold decoding. Code concatenation is also considered in order to provide a further coding gain with a limited increase of the overall complexity. The paper is organized as follows. In the next section, we provide a brief overview of the decoding techniques used for CSOCs, namely majority-logic decoding and its soft-input version, threshold decoding. The proposed FEC schemes for application in the optical channel and numerical results are presented in section 3, along with a discussion on the VLSI implementation. Finally, conclusions are drawn in section 4.

2. MAJORITY-LOGIC AND THRESHOLD DECODING OF CSOCS

A CSOC is a convolutional code for which no two parity equations include the same two bits. Any code that satisfies this definition will have the property that a set of estimates *orthogonal* to an error bit can be obtained directly from some syndrome symbols.*

Using this property of CSOCs, simple decoding algorithms, such as those described in this section, can be identified.[3] Good CSOCs were obtained by Massey,[7] Robinson and Bernstein,[13] and Wu.[8–10] A minor drawback of these codes is that the algebraic constraint prevents, for a given constraint length, from the possibility of high coding gains, or, equivalently, in order to achieve high coding gains, large values of the code constraint length have to be chosen.

In order to illustrate the decoding techniques for CSOCs, let us consider, without loss of generality, a rate 1/2 code. Majority-logic decoding is a hard-input hard-output (HIHO) technique which operates on the syndrome values. At each decoding step, after an information bit i_n and a parity bit p_n have been received and hard-quantized, the decoder calculates the corresponding syndrome value s_n (using also the previous received information bits, according to the code generator). A suitable set of J syndromes† is used to obtain a decision on the error e_{n-d} related to a previous information bit i_{n-d}. Mathematically, the rule takes the form

$$e_{n-d} = 1 \quad \text{if and only if} \quad \sum_{j=1}^{J} s_{n-l_j} \geq \left\lceil \frac{J}{2} \right\rceil \tag{1}$$

where $\lceil x \rceil$ denotes the smallest integer greater than or equal to x and l_j is the delay corresponding to the j-th syndrome value which has to be used into the decision on e_{n-d}. Bit estimates are then properly fed back into the syndrome register to improve the reliability of the syndrome bits.

Example: As an example of a CSOC of rate 1/2 with minimum Hamming distance $d_H = J + 1 = 4$, let us consider the following simple systematic code.[13] This code emits the input information bit i_n along with a parity bit $p_n = i_n \oplus i_{n-2} \oplus i_{n-3}$, where $\oplus$ denotes modulo-2 addition. It is easy to verify that the following orthogonal $J + 1 = 4$ estimates of the information bit i_{n-3} may be constructed:

$$\begin{aligned} &\hat{i}_{n-3} \\ &\hat{p}_n \oplus \hat{i}_n \oplus \hat{i}_{n-2} \\ &\hat{p}_{n-1} \oplus \hat{i}_{n-1} \oplus \hat{i}_{n-4} \\ &\hat{p}_{n-3} \oplus \hat{i}_{n-5} \oplus \hat{i}_{n-6} \end{aligned} \tag{2}$$

where $\hat{i}_n$ and $\hat{p}_n$ denote the received information and parity bit after hard-quantization, respectively. These orthogonal estimates may be used to decode, with a majority decision, the information bit i_{n-3}. Equivalently, defining the syndrome

$$s_n \stackrel{\triangle}{=} \hat{p}_n \oplus \hat{i}_n \oplus \hat{i}_{n-2} \oplus \hat{i}_{n-3} \tag{3}$$

a decision on the error e_{n-3} related to i_{n-3} may be taken, with a majority decision, using the following $J = 3$ syndrome values: s_n, s_{n-1}, and s_{n-3}. The decision rule takes the form

$$e_{n-d} = 1 \quad \text{if and only if} \quad s_n + s_{n-1} + s_{n-3} \geq 2\,. \tag{4}$$

A majority-logic decoder can be readily configured to accept soft-inputs (SI). The corresponding SIHO (soft-input hard-output) algorithm, called threshold decoding, is based on the following strategy.[14,15] A reliability value, taken from a set of M values,‡ is associated to each received information or parity bit. This reliability value depends on the distance of the received sample from the hard-quantization threshold. Using these reliability values, we may

*A set of linear combinations of error bits is said orthogonal with respect to one of the error bits if that bit appears in each equation of the set and no other bit appears in more than one equation.

†Parameter J is related to the minimum Hamming distance d_H of the code by the relation $d_H = J + 1$.

‡M is the number of levels used in the quantization.

associate to the syndrome value s_n the weight w_n as the minimum of the reliability values related to the information and parity bits involved in the computation of s_n, excluding i_{n-d}. The detection strategy becomes

$$e_{n-d} = 1 \quad \text{if and only if} \quad \sum_{j=1}^{J} w_{n-l_j} s_{n-l_j} \geq T \tag{5}$$

and the threshold T is defined as

$$T \triangleq \frac{1}{2} \sum_{j=1}^{J} w_{n-l_j} + \frac{w'_{n-d}}{2} \tag{6}$$

where w'_{n-d} is the reliability value associated to the information bit i_{n-d}.[14,15]

In order to provide soft-output (SO), threshold decoding may be enhanced simply by associating to each decision a reliability value related to

$$\left| \sum_{j=1}^{J} w_{n-l_j} s_{n-l_j} - T \right| . \tag{7}$$

In this way, we obtain a SISO module that can be used as inner decoder in a serial concatenation.

Majority-logic and threshold decoding algorithms, described in this section, exhibit a very good performance, almost equal to the optimal one obtainable with hard- and soft-inputs, respectively, and are characterized by a fixed delay.

3. PROPOSED FEC SCHEMES AND NUMERICAL RESULTS

In this section, we discuss the application of CSOCs and the described decoding techniques to high-speed optical transmissions with particular reference to the problems related to the implementation of the decoder on a single integrated circuit (IC).

We first consider a rate 9/10 CSOC with $J = 11$.[8] This code is decoded using majority-logic and threshold decoding. In the latter case, a 2-bit quantization is considered. The performance is assessed by means of computer simulation in terms of bit error rate (BER) versus Q_b, the "factor Q" normalized per information bit, that is $Q_b = Q/R$ where R is the rate of the code.

The performance is shown in Fig. 1 and compared with that of a RS(255,239) code and an uncoded system. We may observe that, whereas in the case of majority-logic decoding the loss with respect to the RS code is of 0.3 dB at a BER of 10^{-7}, with threshold decoding we obtain a gain of 0.4 dB.

A significant gain with respect to the RS(255,239) may be obtained by concatenating the considered CSOC, used as inner code, with another CSOC of rate 8/9 and $J = 11$.[8] In order to reduce the overall decoder complexity, a direct concatenation without interleaving is considered. Several decoding schemes are analyzed. In the first one, majority-logic decoding is adopted for both the inner and the outer decoder. Therefore, each decoder is HIHO. As may be observed from Fig. 1, with respect to the RS code this scheme may give a coding gain for very low BER. In the second scheme, threshold decoding is used for the inner decoder (SIHO) and majority-logic decoding for the outer decoder (HIHO). In this case, a gain of 1.3 dB may be obtained with respect to the RS code at a BER of 10^{-7}. However, this gain gets larger for lower BER. A gain of 1.5 dB may be obtained using threshold decoding for both the inner and the outer decoder. In this case, the inner decoder has to provide soft-outputs to the outer one.[§] In all the schemes based on threshold decoding, an additional gain of 0.3 may be obtained using a 3-bit quantization. This very good performance of the concatenated schemes without interleaving relies on the property of CSOCs of not producing additional and bursty errors at the decoder output when the capability of the decoder is exceeded.

As a final remark, we discuss the VLSI implementation of the considered decoding schemes. In Table 1, transistor and gate counts are shown in the case of some recently proposed VLSI architectures.[16–18] Different quantizations are considered for threshold decoders. Transistor count is used for full custom Application Specific Integrated Circuit (ASIC) implementation, whereas gate count is used to evaluate the complexity of a gate array implementation. In practice, due to the extremely high decoder clock rate required in a multigigabit-per-second transmission, N

[§]In this case, we have an inner SISO decoder and an outer SIHO decoder.

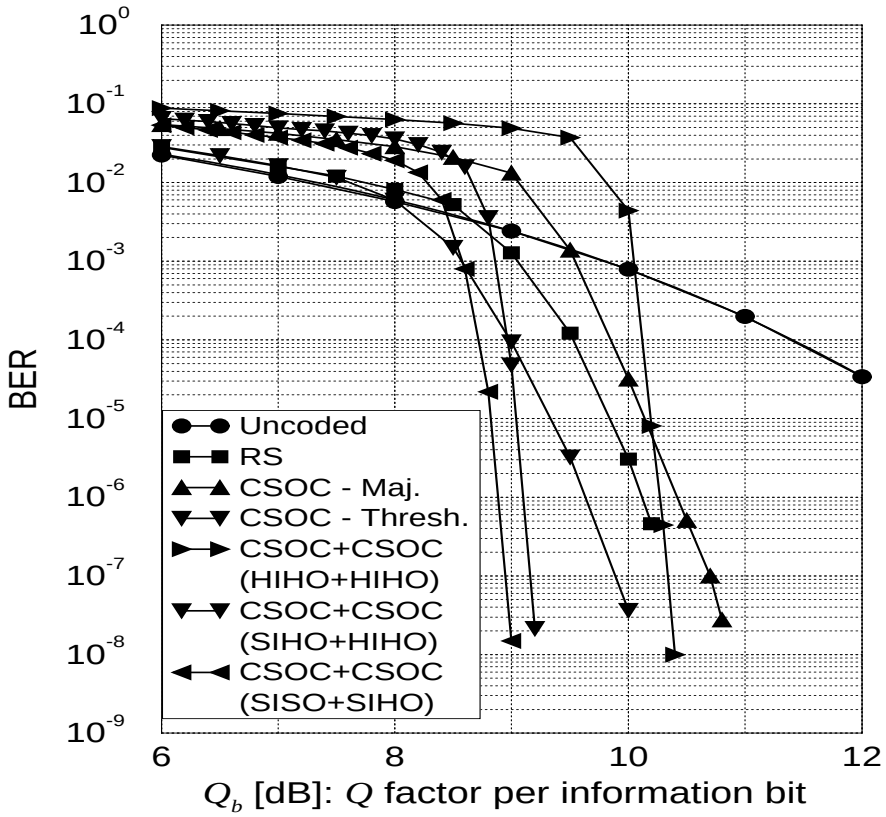

Figure 1. BER of the proposed FEC schemes.

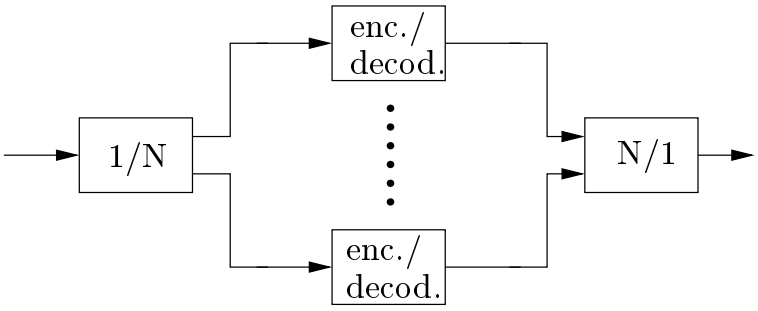

Figure 2. Pipelined structure of encoder and decoder.

encoding and decoding operations have to be pipelined as in Fig. 2. For example, if a 80 MHz clock is used, $N = 12$ CSOC encoders/decoders with rate 9/10 must be pipelined in order to achieve a 10 Gb/s transmission. In this case, majority-logic decoding exhibits an overall complexity of 144,000 gates. Since as of today a limit of $2 \cdot 10^6$ gates can be placed on a single IC, the proposed majority-logic decoding appears therefore as a viable solution for optical transmissions up to 40 Gb/s, whereas a 2-bit threshold decoder is similarly feasible at 10 Gb/s by using a clock rate of 160 MHz. Note that with a clock rate of 80 MHz, a RS(255,239) requires pipelining of 16 decoders and consequently an overall complexity of 420,000 gates instead of 144,000. We point out however, that comparing the gate counts for a given clock rate may not provide a complete picture since majority-logic decoders and threshold decoders are simpler than a RS decoder and therefore, due to their simplicity, may use a higher clock rate up to 160

MHz with a lower degree of pipelining, further reducing the gate needs.

Table 1. Complexity of the proposed decoders for the considered CSOC with rate 9/10.

Decoder type	Transistors	Gates
Majority-Logic	10,000	12,000
Threshold (2-bit quantizat.)	250,000	300,000
Threshold (3-bit quantizat.)	500,000	600,000

4. CONCLUSIONS

Some simple forward error correction schemes based on convolutional self-orthogonal codes and majority-logic and threshold decoding have been analyzed. Coding gains in the range of 1.3 to 1.8 dB with respect to the Reed-Solomon (255,239) code may be obtained through concatenated schemes without interleaving. VLSI implementation has also been discussed showing that the proposed schemes may be implemented on a single integrated circuit to operated at high data rates.

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