

demonstrated. The measured values agree well with the calculated results, and excellent return loss and radiation pattern are realised. Electromagnetically coupled CPW, therefore, can be applied as a candidate for a planar antenna feeding system.

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SELF-CLOCKING SCHEME FOR BIT SYNCHRONISATION IN ULTRAFAST PACKET SWITCHING TRANSPARENT OPTICAL NETWORKS

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Indexing terms: Optical communication, Synchronisation

A challenging issue in ultrafast packet switching transparent optical networks is fast acquisition of synchronisation at the bit level for packet demultiplexing. In the Letter a novel scheme is proposed, in which a timing reference is transmitted along with each data packet in the form of a clock comb. This comb is extracted at each node reached by the packet for header recognition and, at the destination, for reading of that particular packet. The synchronisation problem is solved with no need for a phase locked loop, at the expense of an increased effective packet length.

Transparent optical networks can achieve very high throughput by efficiently using the fibre bandwidth. For this purpose, either many wavelength division multiplexed (WDM) channels at low electronic bit rates, or a few WDM channels at ultrafast optical bit rates can be used.

Ultrafast channels at bit rates approaching 100 Gbit/s need all-optical techniques for packet decompression. All-optical sampling gates have been used to match the ultrafast optical bit rate to the lower electronic bit rate [1, 2]. A specific bit in the packet is extracted by logically ANDing it with a synchronised optical sampling pulse and detecting the result by a fast photodiode. Synchronisation precision requirements between the data and sampling pulse place an upper limit on the highest bit rate achievable over a single channel.

Bit synchronisation is typically achieved by acquiring the timing at each node by means of a phase locked loop (PLL). Optical PLLs suitable for ultrahigh bit rates have recently been proposed and demonstrated [3-5] to demultiplex time division multiplexed (TDM) data streams. In packet switching networks, however, the timing acquisition has to be performed on a packet by packet basis, and this operation should be performed in a small fraction of the packet duration. At ultrahigh bit rates, this implies very short acquisition times.

In optical PLLs, the phase detection function must be implemented all-optically, because extremely short time differences must be resolved. Even though all-optical phase detectors are intrinsically very fast, a very high number of signal pulses are needed to build an appreciable phase-error signal [3] or to obtain a sufficiently large lock-in range [5], so that

the acquisition time might become exceedingly long compared to the packet duration. Moreover, a fast acquisition time implies higher sensitivity to noise in the locking mode.

In this Letter an alternative approach to the bit synchronisation problem is proposed, that makes use of a differential or self-clocking technique [6] to avoid the use of a PLL. Timing information is transmitted as a clock comb before each data packet to form a self-clocking optical packet. The clock comb is extracted at each visited node to provide local sampling pulses for header recognition, and demodulation at the destination.

As shown in Fig. 1, a copy of the incoming self-clocking packet is sensed by a photodetector to trigger the switch S for

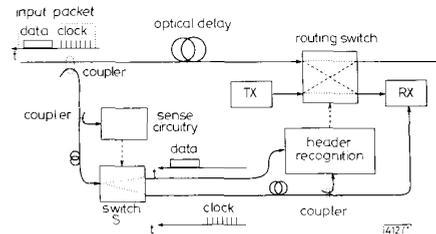


Fig. 1 Node block diagram with sampling clock extraction
TX: transmitter, RX: receiver

a time long enough to spatially separate the clock segment from the data segment. The switch is normally set on the data branch to avoid interference on the clock line and is commuted on the clock branch only at the passage of the clock comb. A guard band δ exists between clock and data to accommodate the time uncertainty in the sense circuitry and the commuting time of the switch. Data and clock are fed to the header recognition block. An electrical control signal is sent to the routing switch to extract the optical packet from the network when its address matches the node's address. The absorbed packet is routed to the receiving block (RX) together with the clock comb for packet demodulation. The details of the proposed self-clocking packet structure are shown in Fig. 2. The data segment has the spread header structure introduced in Reference 7 that allows the number of optical sampling gates needed to decompress the packet to be minimised.

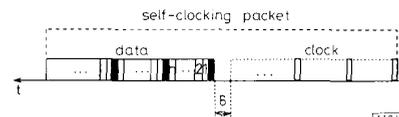


Fig. 2 Self-clocking packet structure with spread header
Header bits are shown hatched

Denoting by R the optical bit rate, the data segment can be thought of as an interleaving of $n + 1$ very low duty cycle data streams at lower bit rate $R_c = R/(n + 1)$, each consisting of h short ON/OFF pulses, for a total packet length of $h(n + 1)$ bits. The packet header, shown hatched in the Figure, is the first of these data streams, regularly spread across the packet.

The sampling clock comb is itself a stream of all 1s at rate R_c and is transmitted before the original packet, at the same wavelength.

As shown in Fig. 3, by sliding a suitably delayed version of the optical clock comb over the data packet, each of the $n + 1$ interleaved data streams can be sampled out of the packet by means of an optical AND gate and sent onto a fast photodiode.

If n is large enough, the data streams have bit rate R_c low enough to be handled by a parallel bank of $n + 1$ conventional direct detection optical receivers, of which n are in the RX block and only one in the header recognition block [7]. Note that the alignment precision between clock and data is only limited by the precision with which the optical delay can be adjusted.

Because clock and data are at the same wavelength, the AND operation could be implemented with soliton trapping gates

[8] or with a nonlinear-optical loop mirror in the two-polarisation-state configuration [9]. Gates based on the

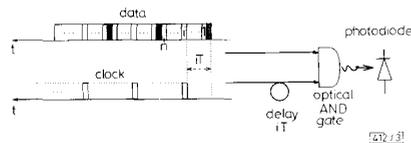


Fig. 3 Delay-and-multiply optical sampling

nonlinear-optical loop mirror in the two-wavelength configuration [10] and on four wave mixing [11] could also be used, if a fast wavelength shifter were provided after the switch S in the clock branch.

For ease of presentation, the clock segment length in Figs. 2 and 3 was set equal to the data segment length. However, only a part of the clock segment needs to be transmitted, and the complete clock comb can be locally reconstructed on the clock branch after the switch S by splitting and delaying the clock pulses, as shown in Fig. 4. The length of the partial

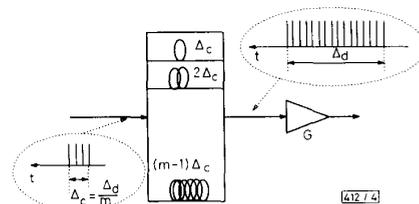


Fig. 4 Local reconstruction of complete sampling clock comb

Δ_d = data segment length, Δ_c = partial clock segment length

clock segment will be a tradeoff between hardware complexity and the required total power of the reconstructed sampling comb. Referring to Fig. 4, if m is the number of delay lines, and the guard time δ is neglected, the clock overhead increases the total packet length by a factor $1/m$, so that for instance a value as low as $m = 8$ already gives a clock overhead below 13%. Amplification is provided next to restore the necessary clock sampling power. Note that even a PLL would need a packet overhead whose length is inversely proportional to its acquisition time.

To gain a feeling of the performance of the proposed self-clocking scheme, reference can be made to ultrafast soliton transmission. When ultrashort soliton pulses are employed in a packet switching network, the dominant noise source is the jitter of the pulse arrival time due to amplified spontaneous emission (ASE) noise introduced by the optical amplifiers placed at each node and to the soliton self-frequency shift (SSFS) due to Raman scattering*. The SSFS causes a time shift of the pulse arrival time which is the same for all bits in the packet. It is thus totally eliminated by the proposed differential technique. The ASE noise, instead, is broadband, i.e. each pulse in the packet is independently affected. The sampling jitter variance is thus twice the variance of the arrival time jitter due to ASE only, because of the differential technique employed.

If an optical PLL with fast acquisition time were available, the sampling jitter between clock and bit pulse in the optical AND gate would be the sum of a highpass filtered version of the arrival time jitter affecting the data bits and of the PLL residual tracking jitter. The self-clocking scheme should still be preferable to the PLL whenever the arrival time jitter variance is lower than the residual PLL jitter variance. More-

* BONONI, A., FORGHIERI, F., and PRUCNAL, P. R.: 'Design and channel constraint analysis of ultra-fast multihop all-optical packet switching networks with deflection routing employing solitons', submitted to *J. Lightwave Technol.*

over, its low hardware complexity would make it an attractive solution even if low-jitter fast PLLs become available.

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ULTRALOW LASER THRESHOLD AND HIGH SPEED InGaAs-GaAs-InGaP BURIED HETEROSTRUCTURE STRAINED QUANTUM WELL LASERS FOR OPTICAL INTERCONNECTS

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Indexing terms: Semiconductor lasers, Lasers

The Letter reports ultralow laser threshold and high speed InGaAs-GaAs-InGaP buried heterostructure strained quantum well lasers entirely grown by a three step MOVPE process for computer interconnects. Uncoated 350 μm -long buried heterostructure lasers show an extremely low laser threshold of 0.8 mA and a high slope efficiency of 0.41 mW/mA per facet both measured CW at RT, and a high relaxation oscillation frequency of 5.1 GHz at a bias current of 4 mA.

For semiconductor lasers to be employed in computer interconnects, their characteristics should include submilliwatt laser threshold and very high speed modulation [1]. Until recently, ultralow laser threshold (as low as 1 mA without coatings) and high speed operation have been exclusively realised with (In)GaAs-AlGaAs buried heterostructure (BH) quantum well lasers [2]. These devices have been fabricated by a hybrid growth technique using both molecular beam