Demonstration of an optically transparent ATM packet switch node

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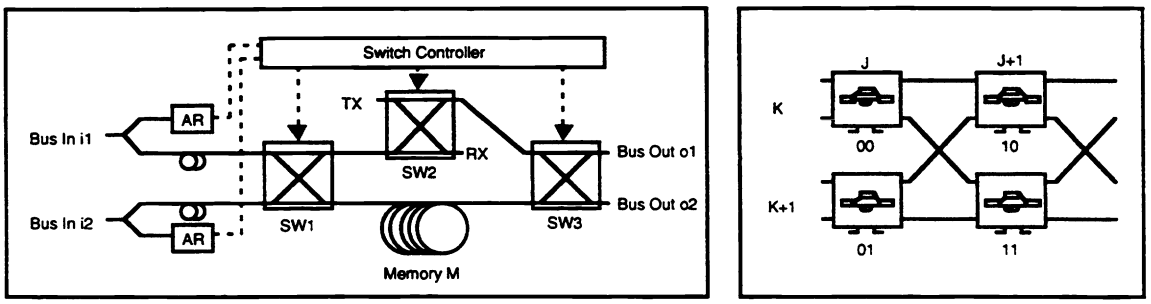
ABSTRACT

We report on the development of a transparent optical node at 1.3 μm wavelength for an ATM packet switch operating at 1.24416 Gbit/s header recognition rates. The node takes advantage of the high-speed performance of optoelectronic components to alleviate potential bottlenecks resultant from optical to electrical conversions experienced in non-transparent packet switching architectures. The node is intended for use in two-connected, slotted networks, is self clocking and has drop/add multiplexing, buffering and routing capabilities.

1. INTRODUCTION

Extremely high bit rates can be used in transmission by each node in space switching transparent optical networks, since nodes are connected by dedicated fiber links. The electronic control of the switching nodes may limit the bit rate since routing computations must be performed within a packet's duration. Extremely simple node structures are thus desirable that have low loss and simple control, while still providing good throughput-delay performance.

A new node structure shown in Figure 1a with a single transmitter TX and receiver RX employing deflection routing[1] is proposed here for two-connected, slotted networks. Only three 2x2 optical switches are used, the theoretical minimum of all possible single-buffer all-optical node schemes, for a node capable of accessing/receiving either channel. Without the one-packet fiber delay loop memory M, it would be a 3x3 completely non-blocking switch.[2]



a) b)

Figure 1. a) Schematic diagram of transparent optical node. b) Node configuration for routing experiment.

Packets entering the node at i1 or i2 and contained in M are perceived by the controller in one of five possible ways: empty (E), for the node (FN), caring to exit on output o1 (C1), caring to exit on output o2 (C2), or don't care (DC), i.e., both outputs provide equivalent shortest-paths to their destination. Deflections occur when packets at the input of SW3 vie for the same output. When i1 and i2 are FN, one is missed. The objective of the controller is to maximize the node's throughput by minimizing the number of deflections. Switch SW2 is just for absorption/injection, and routing switch

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SW3 is controlled with a simple non-priority hot-potato routing[1] of its input packets. The description of the switch settings ("i?" stands for "one of the two inputs") is as follows:

if (i1=i2) ⇒ Randomize SW1
elseif (i?=FN) ⇒ set SW1 to receive it
elseif ((i1,i2)=C1,C2) or (C2,C1)) and (M=E or DC) ⇒ Randomize SW1
elseif (i?=E) and (TX=full) ⇒ set SW1 to receive E
elseif (M,i?) = ((C2,C2) or (C1,C1)) ⇒ store that input
else store E's or DC's

Absorption of FN packets is done first. Line 3 accounts for the fact that two care non-conflicting packets cannot be routed out directly, as memory cannot be bypassed. Empty slots are routed to TX for possible injection. Conflicts with the memory are resolved by storing the conflicting input. E's and DC's are stored when possible to avoid deflections at the next slot.

The throughput vs. offered load (i.e., the probability of having a packet ready at TX at each clock) for a 64-node ShuffleNet in uniform traffic has been theoretically evaluated.[3] In comparison with the throughput of nodes with no delay loop memory M (i.e., hot-potato routing) and of nodes with infinite-buffers (i.e., store-and-forward S&F) at full load, the proposed node structure yields 71% of the maximum S&F throughput while the node with no delay loop memory yields only 52%. This is a 37% increase in throughput at the cost of building only a slightly more complicated controller.

2. EXPERIMENT

The transparent optical node illustrated in Figure 1a was constructed with three Crystal Technology SW313P $LiNbO_3$ electro-optic crossbar switches (SW1, SW2 and SW3) and a length of optical fiber for the purposes of routing, buffering and drop/add multiplexing of incoming packets. The $LiNbO_3$ switches were measured to have average fiber-to-fiber losses of -6.4 dB when connected in the configuration of Figure 1a for an overall throughput loss of -19.2 dB for a packet traversing all three switches. Such a loss can be reduced by 3 to 6 dB by improving the fiber splice connections within the node structure. Power levels can be restored using an optical amplifier placed at the bus output ports of the node. However, the noise introduced by optical amplifiers imposes an upper limit on the maximum usable bit rate [4]. For these experiments a four node banyan interconnect as shown in Figure 1b was assumed for routing purposes. Thus, valid binary packet destination addresses JK for this interconnect are 00, 01, 10 and 11.

Address recognition is performed at input port i1 by tapping off a portion of the incoming signal power with a -3 dB splitter and detecting the address signals of interest. The power in the address recognition portion of the signal is sent through an optical fiber 1x4 divider and delay structure for parallel detection of four bits of information in the packet header field. ATM packet structures consisting of a 5 byte header field and 48 byte data field were used. A portion of a typical 1.24416 Gbit/s NRZ input packet is shown in Figure 2. These data are optical pulses detected with an AT&T 127B InGaAs avalanche photodiode and measured with a Tektronix 11801 digitizing sampling oscilloscope and an SD-26, 20 GHz bandwidth sampling head.

Every incoming packet structure, including empty packets, begins with a two-bit-wide framing pulse in the header field. The framing pulse is used for self-clocking of packets entering the node and to maintain overall network synchronization. Since the framing pulse must be sent with every packet time slot, an address bit E in the header field is used to determine whether or not an empty packet has been sent in the slot. When the destination address bits J or K had digital values of zero they were always surrounded by optical one bits to ensure that a true zero was detected at the 1.24416 Gbit/s data

rate. Prior to entering the node, the packet is buffered by a length of optical fiber while the state of the three $LiNbO_3$ switches is set according to the prioritization algorithm. This address recognition delay stage is 120 ns, 92 ns of which is due to propagation delays in the electronic controller circuitry. The majority of this time, approximately 83 ns, is associated with the setup and hold time requirements of a CMOS programmable logic array used to derive the switch state settings from 2^{14} possible input combinations. These controller inputs are the three-bit destination address information (EJK) of packets at i1, i2, TX and M, as well as the two bit address of the optical node itself.

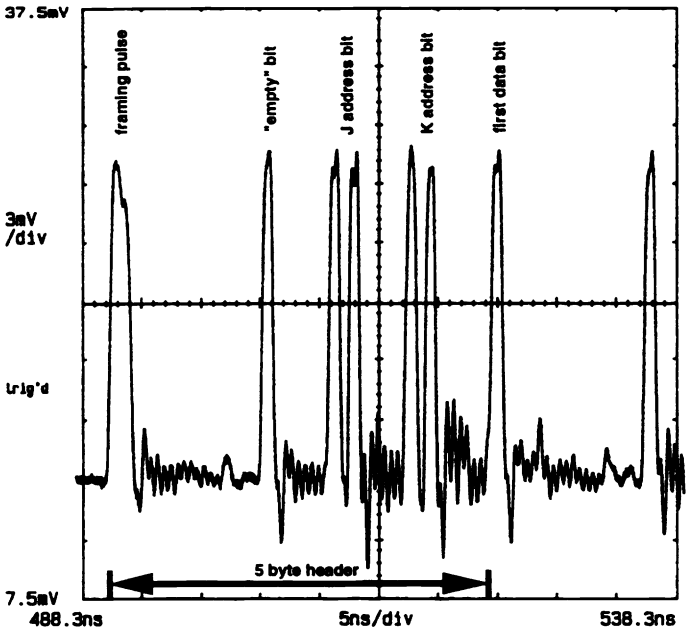

Figure 2. Detected header field of a typical packet.

Experimental results for the switch operating as node address 00 and with empty packets incident at TX are shown in Figures 3a and 3b. Figure 3a is a plot of the series of incoming packets at TX (upper trace), i1 (middle trace) and i2 (lower trace). The data rates for packets at i1 and i2 were 1.24416 Gbit/s and 622.08 Mbit/s, respectively, and have low mark ratios for viewing purposes. Indeed, the data rates in the packet data fields can be multi-Gbit/s. The guardband between packets is 51.44 ns. The empty packets incident at TX have no framing pulse associated with the packet time slot due to unavailability of a third modulatable laser source. The i2 packets all have the same destination address of 101 (*i.e.*, they are all DC packets). The packets incident at i1 have destination addresses 100, 110, 000 and 111, (*i.e.*, they are FN, C1, E, and C2, respectively). The packets detected at the output ports are shown in Figure 3b. The packet with destination address 100 is correctly dropped at RX (upper trace) followed by empty packets from TX, i1 and TX. Packets detected at o1 (middle trace) have destination address 101 from TX, 000 from M via i2, 110 from M via i1, and 000 from M via i2. Packets detected at o2 (lower trace) have destination address 111 from M via i1, 101 from TX, 101 from TX and 101 from TX.

The effect of crosstalk within the node on BER performance was measured at the 1.24416 Gb/s data rate and the results are shown in Figure 4. The baseline (solid line with filled circles) was measured transmitting a pseudorandom 2^{23}-1 bit stream between i2 and o2 with SW1, SW2 and SW3 in the cross state, no signal input to TX or i1, and the memory M disconnected. This removes all instances of crosstalk from arriving at the receiver. The memory M is then connected and PSRB data transmitted on i1 and TX and the effect of crosstalk of BER performance is measured (dashed line with open circles). As can be seen from Figure 4, a penalty of a small fraction of a dB is found.

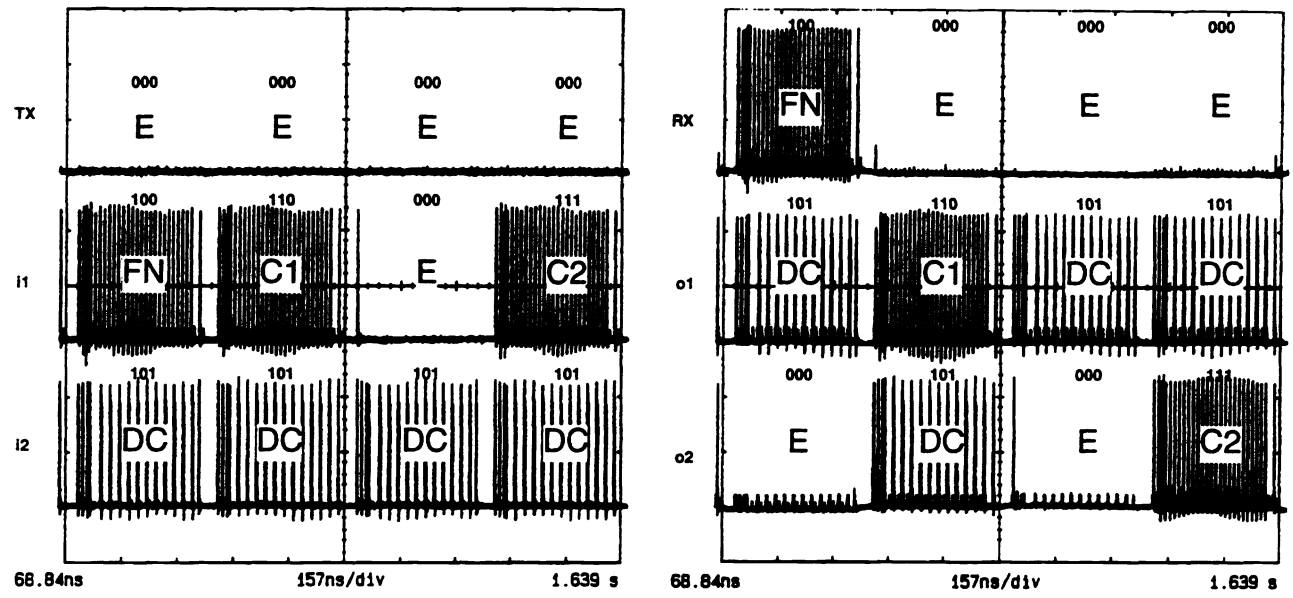

Figure 3. a) Incident packets at input ports TX (upper trace), i1 (middle trace) and i2 (lower trace) with respective destination addresses identified. b) Departing packets at output ports RX (upper trace), o1 (middle trace) and o2 (lower trace) with respective destination addresses identified.

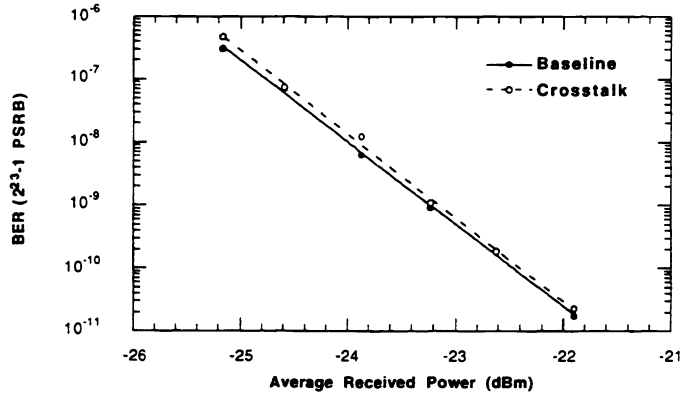

Figure 4. Effect of crosstalk within the node on BER at 1.24416 Gb/s data rates.

3. REFERENCES

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2. F. Forghieri, A. Bononi, and P.R. Prucnal, "Analysis and comparison of hot-potato and single buffer deflection routing in very high bit rate optical mesh networks," to be published in *IEEE Trans. Commun.*
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