3 RUMELHART, D.E., HINTON, G.E., and WILLIAMS, R.J.: 'Learning internal representations by error propagation' *in* RUMELHART, D.E., and MCCLELLAN, J.L., (Eds.), 'Parallel distributed processing: Exploration in the microstructure of cognition. Vol. 1'

1.24416Gbit/s demonstration of a transparent optical ATM packet switch node

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Indexing terms: Optical communication, Asynchronous transfer mode, Packet switching, Optical switches

The authors report the development of a transparent optical node at 1.3μm wavelength for an ATM packet switch operating at 1.24416Gbit/s header recognition rates. The node is intended for use in two-connected, slotted networks, is self-clocking and has drop/add multiplexing, buffering and routing capabilities.

Introduction: Extremely high bit rates can be used in transmission by each node in space switching transparent optical networks, because nodes are connected by dedicated fibre links. The electronic control of the switching nodes may limit the bit rate because routing computations must be performed within a packet's duration. Extremely simple node structures are thus desirable that have low loss and simple control, while still providing good throughput-delay performance.

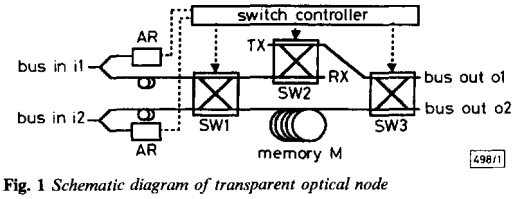

Fig. 1 *Schematic diagram of transparent optical node*

A new node structure shown in Fig. 1 with a single transmitter TH and receiver RX employing deflection routing [1,2] is proposed here for two-connected, slotted networks. Only three 2 × 2 optical switches are used, the theoretical minimum of all possible single-buffer all-optical node schemes, for a node capable of accessing/receiving either channel. Without the one-packet fibre delay loop memory M [3], it would be a 3 × 3 completely non-blocking switch.

Packets entering the node at i1 or i2 and contained in M are perceived by the controller in one of five possible ways: empty (E), for the node (FN), caring to exit on output o1 (C1), caring to exit on output o2 (C2), or don't care (DC), i.e. both outputs provide equivalent shortest-paths to their destination. Deflections occur when packets at the input of SW3 vie for the same output. When i1 and i2 are FN, one is missed. The objective of the controller is to maximise the node's throughput by minimising the number of deflections. Switch SW2 is just for absorption/injection, and routing switch SW3 is controlled with a simple non-priority hot-potato routing [1] of its input packets.

The throughput against offered load (i.e. the probability of having a packet ready at TX at each clock) for a 64-node ShuffleNet in uniform traffic has been theoretically evaluated [4]. In comparison with the throughput of nodes with no delay loop memory M (i.e. hot-potato routing) and of nodes with infinite buffers (i.e. store-and-forward S&F) at full load, the proposed node structure yields 71% of the maximum S&F throughput while the node with no delay loop memory yields only 52%. This is a 37% increase in throughput at the cost of building only a slightly more complicated controller.

Experiment: The transparent optical node illustrated in Fig. 1 was constructed with three Crystal Technology SW313P $LiNbO_3$ electro-optic crossbar switches (SW1, SW2 and SW3) and a length of optical fibre for the purposes of routing, buffering and drop/add multiplexing of incoming packets. The $LiNbO_3$ switches were measured to have average fibre-to-fibre losses of –6.4dB when connected in the configuration of Fig. 1 for an overall throughput loss of –19.2dB for a packet traversing all three switches. Such a loss can be reduced by 3 to 6dB by improving the fibre splice connections within the node structure. Power levels can be restored using an optical amplifier placed at the bus output ports of the node. However, the noise introduced by optical amplifiers imposes an upper limit on the maximum usable bit rate [5]. For these experiments a four node banyan interconnect was assumed for routing purposes. Thus, valid binary packet destination addresses JK for this interconnectare 00, 01, 10 and 11.

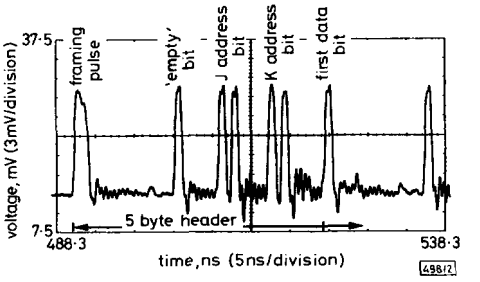

Fig. 2 *Detected header field of typical packet*

Address recognition is performed at input port i1 by tapping off a portion of the incoming signal power with a –3dB splitter and detecting the address signals of interest. The power in the address recognition portion of the signal is sent through an optical fibre 1 × 4 divider and delay structure for parallel detection of four bits of information in the packet header field. ATM packet structures consisting of a 5 byte header field and 48 byte data field were used. A portion of a typical 1.24416Gbit/s NRZ input packet is shown in Fig. 2. These data are optical pulses detected with an AT&T 127B InGaAs avalanche photodiode detector and measured with a Tektronix 11801 digitising sampling oscilloscope and an SD-26, 20GHz bandwidth sampling head.

Every incoming packet structure, including empty packets, begins with a 2-bit-wide framing pulse in the header field. The framing pulse is used for self-clocking of packets entering the node and to maintain overall network synchronisation. Because the framing pulse must be sent with every packet time slot, an address bit E in the header field is used to determine whether or not an empty packet has been sent in the slot. When the destination address bits J or K had digital values of zero they were always surrounded by optical one bits to ensure that a true zero was detected at the 1.24416 Gbit/s data rate. Prior to entering the node, the packet is buffered by a length of optical fibre while the state of the three $LiNbO_3$ switches is set according to the prioritisation algorithm. This address recognition delay stage is 120ns, 92ns of which is due to propagation delays in the electronic controller circuitry. The majority of this time, ~83ns, is associated with the setup and hold time requirements of a CMOS programmable logic array used to derive the switch state settings from 2^{14} possible input combinations. These controller inputs are the 3-bit destination address information (EJK) of packets at i1, i2, TX and M, as well as the 2 bit address of the optical node itself.

Experimental results for the switch operating as node address 00 and with empty packets incident at bus input i2 are shown in Figs. 3 and 4. Fig. 3 is a plot of the series of incoming packets at TX (upper trace), i1 (middle trace) and i2 (lower trace). The data rates for packets at TX and i1 were 622.08Mbit/s and 1.24416Gbit/s, respectively, and have low mark ratios for viewing purposes. Indeed, the data rates in the packet data fields can be multigigabit per second. The guardband between packets is 51.44ns. The empty packets incident at input port i2 have no framing pulse associated with the packet time slot due to unavailability of a third modulatable laser source. The TX packets all have the same destination address of 101. The packets incident at i1 have destination addresses 100, 110, 000 and 111, respectively. The packets detected at the output ports are shown in Fig. 4. The packet with destination address 100 is correctly dropped at RX (upper trace) followed by empty packets from i2, i1 and i2. Packets detected at o1 (mid-

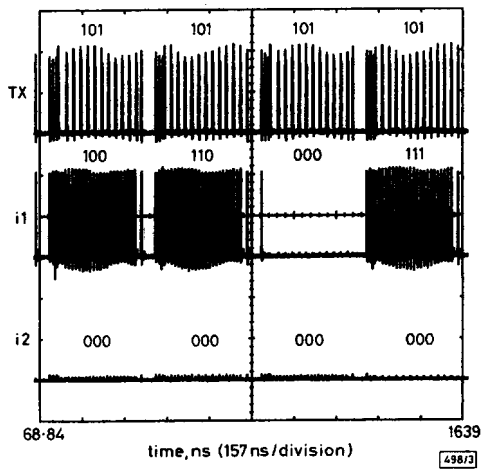

Fig. 3 *Incident packets at input ports TX, o1 and o2 with respective destination addresses identified*

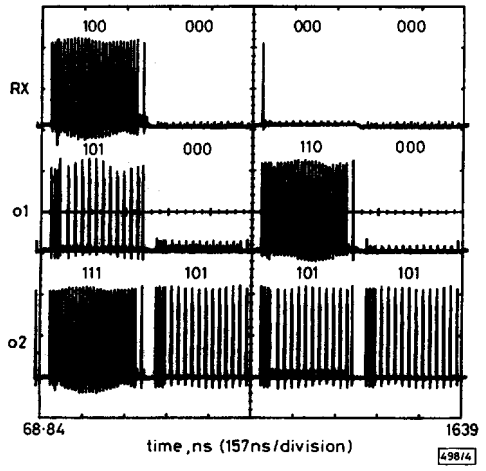

Fig. 4 *Departing packets at output ports RX, o1 and o2 with respective destination addresses identified*

dle trace) have destination address 101 from TX, 000 from M via i2, 110 from M via i1, and 000 from M via i2. Packets detected at o2 (lower trace) have destination address 111 from M via i1, 101 from TX, 101 from TX and 101 from TX.

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References

1 BARAN, P.: 'On distributed communications networks', *IEEE Trans. Commun. Syst.*, 1964, pp. 1–9

2 BLUMENTHAL, D.J., CHEN, K.Y., MA, J., FEUERSTEIN, R.J., and SAUER, J.R.: 'Demonstration of a deflection routing 2 × 2 photonic switch for computer interconnects', *IEEE Phot. Tech. Lett.*, 1992, **4**, (2), pp. 169

3 FORGHIERI, F., BONONI, A., and PRUCNAL, P.R.: 'Analysis and comparison of hot-potato and single buffer deflection routing in very high bit rate optical mesh networks', *IEEE Trans. Commun.*,, (to be published)

4 BONONI, A., and PRUCNAL, P.R.: 'Minimum-loss node structures for deflection routing transparent optical networks', Proc. OFC'94, 1994, San Jose, CA, Paper WI5

5 BONONI, A., FORGHIERI, F., and PRUCNAL, P.R.: 'Design and channel constraint analysis of ultra-fast multihop all-optical networks with deflection routing employing solitons', *J. Lightwave Technol.*, 1993

Effect of normal mode loss in nonlinear optical loop mirror switching

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Indexing terms: Nonlinear optical loop mirrors, Optical switching

The effect of normal mode loss in nonlinear optical loop mirror (NOLM) switching is investigated. It is shown for both CW square and soliton pulse inputs that an unbalanced mode loss shifts the NOLM transmission coefficient with respect to reflection, and that the NOLM excess loss has sinusoidal dependence in the input pulse energy.

The potential of nonlinear optical loop mirrors (NOLM) devices for time-domain, high-speed (10–100Gbit/s) signal processing is now well recognised [1–3]. In communications system applications, important parameters are the NOLM switching power, switching efficiency and extinction ratio. We investigate here the perturbative effect of normal mode loss on such parameters, which had not been taken into account so far in NOLM analysis, and apply the results to the case of CW square and soliton pulses self-switching.

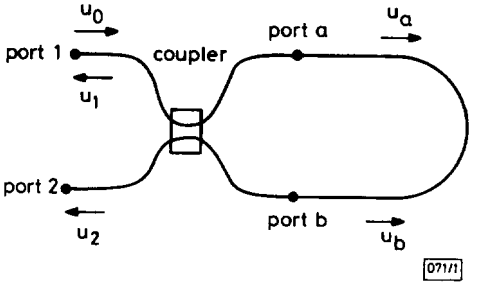

Fig. 1 *Sagnac interferometer*

Consider first the coupler shown in Fig. 1. Let u_0 be the signal field amplitude at input port 1. From the normal mode theory of [4], the output fields at ports a and b are given by $u_a = u_0(\gamma_s e^{i\phi} + \gamma_a e^{-i\phi})/2$ and $u_b = u_0(\gamma_s e^{i\phi} - \gamma_a e^{-i\phi})/2$, where γ_s and γ_a represent the amplitude transmission of the coupler's symmetric and antisymmetric modes, and 2ϕ represents an unspecified relative phase difference. We express here this result under the more explicit form:

$$u_a = u_0\sqrt{\left(\frac{\gamma_s+\gamma_a}{2}\right)^2 - \gamma_s\gamma_a\sin^2\phi} \equiv u_0\sqrt{\alpha_{//}} \quad (1)$$

$$u_b = u_0\sqrt{\left(\frac{\gamma_s-\gamma_a}{2}\right)^2 + \gamma_s\gamma_a\sin^2\phi}\,\exp(i\delta) \equiv u_0\sqrt{\alpha_\times}\exp(i\delta) \quad (2)$$

where $\alpha_{//}$ and $\alpha_\times$ are defined as the power coupling ratios for straight-through and crosscoupling. In eqn. 2, the phase difference δ is given by $\delta = \pi/2 - \varepsilon = \text{Arctan}[2\gamma_s\gamma_a\sin(2\phi)/(\gamma_s^2 - \gamma_a^2)]$ [4]. When the normal mode transmission (or loss) is balanced ($\gamma_s = \gamma_a = \gamma$), eqns. 1 and 2 yield the generic relations $\alpha_\times + \alpha_{//} = \gamma^2$ and $\delta = \pi/2$. In particular, $\phi = \pi/4$ corresponds to a 50:50 coupler, as $\alpha_\times = \alpha_{//} = \gamma^2/2$. Consider next a coupler with unbalanced normal mode loss ($\gamma_s \neq \gamma_a$). We find then that $\alpha_\times + \alpha_{//} = (\gamma_s^2 + \gamma_a^2)/2$, and $\delta \neq \pi/2$. A 50/50 coupler is also achieved for $\phi = \pi/4$, but the two normal modes are not in exact quadrature ($\delta \neq \pi/2$). Consider next the Sagnac interferometer of Fig. 1. Using eqns. 1 and 2, we obtain