WI5 **2:00 pm**

Minimum-loss node structures for deflection-routing transparent optical networks

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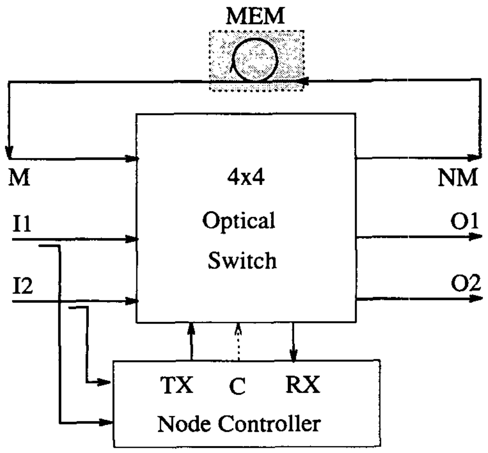
Extremely high bit rates can be used in transmission by each node in space-switching transparent optical networks since nodes are connected by dedicated fiber links. The noise introduced by optical amplifiers imposes an upper limit on the maximum usable bit rate.[1] The electronic control of the switching nodes may also limit the bit rate since routing computations must be performed within a packet's duration. Extremely simple node structures are thus desirable, these node structures have low loss and simple control while still providing good throughput-delay performance.

New node structures with a single transmitter/receiver (TX/RX) using single-buffer deflection routing[2] are proposed here for two-connected slotted multihop networks.



WI5 **Fig. 1.** General shared-memory optical-node structure.

A shared-memory optical node structure is shown in Fig. 1. The node consists of a 4 × 4 optical switch capable of routing flow-through packets from inputs I1, I2 and local packets from the TX and the optical buffer M onto outputs O1, O2 to the RX and back to the optical buffer NM. The buffer is a one-packet fiber delay loop. No amplification is used in the loop. The node controller reads the header of incoming packets and, by taking into account the contents of the TX and M, properly sets the switch electrical controls C.

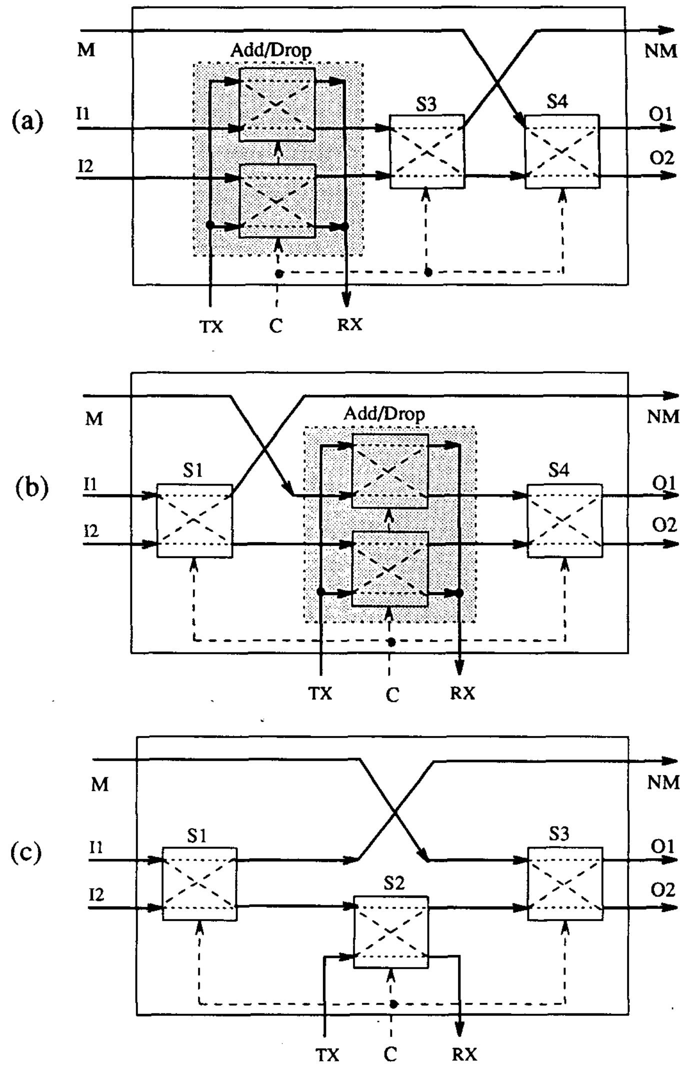
Packets in I1, I2, M at each slot can be empty, can be destined to the node (FM), can be caring to exit on output O1 or on output O2, or can be *don't care* when both outputs provide equivalent shortest paths to their destination. Unavoidable deflections occur when packets in I1, I2, M care for the same output. When I1, I2, M are all FM, one of them must be routed out and is missed. It will come back at a later time.

The objective of the controller is to maximize the node's throughput by minimizing the number of deflections and misses, given the set of permutations allowed by the 4 × 4 switch.

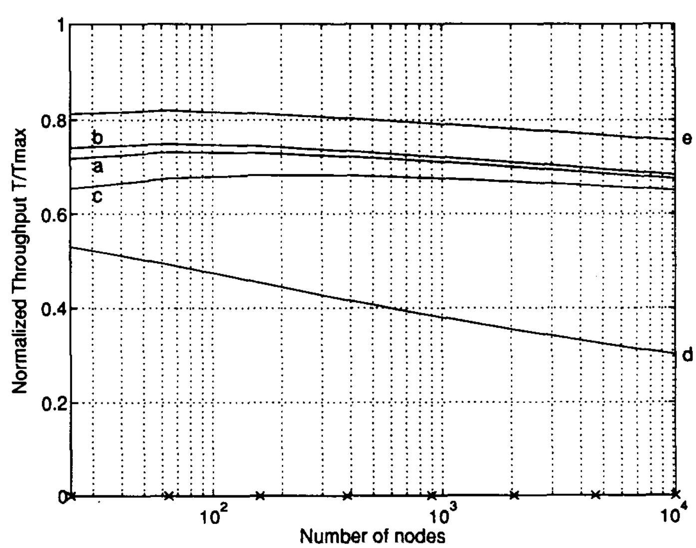
The most flexible control is obtained with a nonblocking optical switch. $LiNbO_3$ optical switches can be used as building elements. Six 2 × 2 switches are required to form a 4 × 4 nonblocking switch.[3]

Figure 2 shows three new solutions for the 4 × 4 node switch. Scheme (a) is the single-receiver version of the node proposed in Ref. 4. Two input switches form the add/drop block for local traffic. Switches S3, S4 form the buffering/routing block. The buffer is shared by I1 and I2, but it cannot be accessed by the receiver. Scheme (b) swaps the add/drop block and the buffer access switch, so that the buffer becomes available to the RX and misses can be reduced. One switch can be removed as shown in scheme (c). Switches S1 and S2 now form the add/drop block, but S1 is also used to access the memory. Only three 2 × 2 optical switches are used, the theoretical minimum for a node capable of transmitting/receiving on either channel.

Efficient control algorithms have been found for all of these structures. A ShuffleNet topology[5] has been chosen to compare their performances. Figure 3 shows the full-load node throughput normalized to the maximum theoretical value obtained for infinite buffers (i.e., when no deflections or misses occur) versus network size. Curve e refers to the nonblocking structure, curves a, b, and c refer to the schemes of Fig. 2, and curve d refers to scheme (c) when no buffer is present. This



WI5 **Fig. 2.** Low-loss configurations of the 4 × 4 optical switch.



WI5 **Fig. 3.** Normalized full-load throughput versus network size in a ShuffleNet topology.

corresponds to hot-potato routing.[2] Scheme (b) performs better than scheme (a) since misses are reduced. There is little difference in performance among the single-buffer structures, which achieve 70–80% of the maximum throughput for networks with as many as 10 000 nodes. The unbuffered structure throughput instead quickly degrades with increasing network size.

The nonblocking switch scheme provides the highest throughput. However, buffered packets might need to cross the 4 × 4 switch many times, each time crossing three 2 × 2 switches. The power loss on such buffered packets could turn out to be unacceptably high, and amplification in the loop might be necessary. The great advantage of the other structures is to have the number of 2 × 2 switch crossings per input channel no higher than 3. Most importantly, in schemes (a) and (b) buffered and unbuffered packets will experience the same loss.

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